




IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Brian Boles et al.  
Serial No.: 09/870,447  
Filing Date: June 1, 2001  
Group Art Unit: 2111  
Examiner: Thomas J. Cleary  
Title: ***VARIABLE CYCLE INTERRUPT DISABLING***

Mail Stop RCE  
Commissioner of Patents  
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I hereby certify that this Information Disclosure Statement is being deposited with the United States Postal Service as Express Mail EV351255161US addressed to: Mail Stop RCE, Commissioner of Patents, Alexandria, VA 22313-1450, on the date shown below.

  
Angela Loding  
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Date

Dear Sir:

**INFORMATION DISCLOSURE STATEMENT**

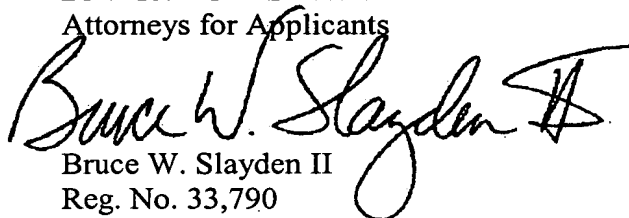
Applicants respectfully request, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the references listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. Copies of the references are enclosed for the convenience of the Examiner. Furthermore, pursuant to 37 C.F.R. §§1.97 (g) and (h), no representation is made that these references are material to the patentability of the present application.



Applicants believe no fees are due with this filing, however, the Commissioner is hereby authorized to charge any fees to Deposit Account No. 50-2148 of Baker Botts L.L.P. in order to effectuate this filing.

Respectfully submitted,

BAKER BOTTS L.L.P.  
Attorneys for Applicants

A handwritten signature in black ink, reading "Bruce W. Slayden II". The signature is stylized with a large, looped "B" and a trailing flourish.

Bruce W. Slayden II  
Reg. No. 33,790

Date: March 15, 2005

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PTO-1449		Application No. 09/870,447		Applicant(s) Brian Boles et al.		
<div style="border: 1px solid black; border-radius: 50%; padding: 10px; display: inline-block;"> <b>Information Disclosure Citation</b>  <b>in an Application</b>  MAR 16 2005  PATENT &amp; TRADEMARK OFFICE </div>		Docket Number 068354.1471		Group Art Unit 2111	Filing Date June 1, 2001	
<b>U.S. PATENT DOCUMENTS</b>						
	<b>DOCUMENT NO.</b>	<b>DATE</b>	<b>NAME</b>	<b>CLASS</b>	<b>SUBCLASS</b>	<b>FILING DATE</b>
A.	3930253	12/30/75	Maida	340	347	1/24/74
B.	5974549	10/26/99	Golan	713	200	3/27/97
C.	6055619	4/25/00	North et al.	713	36	2/7/97
D.	6282637	8/28/01	Chan et al.	712	223	12/2/98
E.	6728856	4/27/04	Grosbach et al.	711	202	6/1/01
F.						
G.						
H.						
I.						
J.						
<b>FOREIGN PATENT DOCUMENTS</b>						
	<b>DOCUMENT NO.</b>	<b>DATE</b>	<b>COUNTRY</b>	<b>CLASS</b>	<b>SUBCLASS</b>	<b>TRANSLATION</b>
						YES    NO
K.	01037424 A	2/89	JP	H03M	001/82	X
L.	0 554 917 A2	8/11/93	EP	G06F	9/26	X
M.	0 855 643 A1	7/29/98	EP	G06F	9/30	X
N.	0 992 888	12/4/00	EP	G06F	9/32	X
O.	0 992 889	12/14/00	EP	G06F	9/32	X
P.	96/11443	4/18/96	WO	G06F	15/78	X
<b>NON-PATENT DOCUMENTS</b>						
	<b>DOCUMENT (Including Author, Title, Source, and Pertinent Pages)</b>					<b>DATE</b>
Q.	Moon B I et al.: "A 32-bit RISC Microprocessor with DSP Functionality: Rapid Prototyping" IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Institute of Electronics Information and Comm. Eng. Tokyo, JP, vol. E84-A no. 5, pages 1339-1347, XP001060025 ISSN: 0916-8508					5/2001
R.	Turley J: "Balancing Conflicting Requirements When Mixing RISC, DSPs" Computer Design, Pennwell Publ. Littleton, Massachusetts, IS, vol. 37, no. 10, pages 46, 48, 50-53, XP000860706 ISSN:0010-4566					10/1998
S.	Levy M: "Microprocessor and DSP Technologies Unite for Embedded Applications" EDN Electrical Design News, Cahners Publishing Co., Newtown Massachusetts, US, no. Europe, pages 73-74, 76, 78-80, XP000779113 ISSN: 0012-7515					3/2/1998
T.	Intel, Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual, , Pages 3-1, 3-2, 3-15, 14-1 to 14-30, 18-7, and 25-289 to 25-292					1995
U.	Intel, Embedded Intel486 Processor Family Developer's Manual, pgs. 2-2, 3-17, 3-37, 4-5, 4-6, 10-1 to 10-12, 12-1 to 12-10					10/1997
EXAMINER				DATE CONSIDERED		
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.						



PTO-1449

Application No.

Applicant(s)

09/870,447

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Group Art Unit

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068354.1471

2111

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**Information Disclosure Citation  
in an Application**

**U.S. PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
A.						
B.						
C.						
D.						
E.						
F.						
G.						
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	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
N.							
O.							
P.							

**NON-PATENT DOCUMENTS**

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
Q.	PCT Search Report based on PCT/US02/16706, 6 pages	Mailed 9/27/02
R.	PCT Search Report based on PCT/US02/16705, 7 pages	Mailed 9/9/02
S.	PCT Search Report based on PCT/US02/16921, 4 pages	Mailed 10/18/02
T.	SPARC, International, Inc., "The SPARC Architecture Manual", Version 8, pp 1 - 303	1992
U.	Weaver, et al., SPARC International, Inc. "The SPARC Architecture Manual", Version 9, pp. xiv, 137, 146-147, 200-204, 221-222, 234-236, 299	1994-2000
V.	Free On-Line Dictionary of Computing (FOLDOC). <a href="http://wombat.doc.ic.ac.uk/foldoc/">http://wombat.doc.ic.ac.uk/foldoc/</a> Search term: program counter	1995

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.